

HEF4894B

12-stage shift-and-store register, LED driver

Rev. 04 — 27 August 2008

Product data sheet

1. General description

The HEF4894B is a 12-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input (D) to the parallel LED driver outputs (QP0 to QP11). Data is shifted on positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the output whenever the output enable (OE) input signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of HEF4894B devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading HEF4894B devices when the clock has a slow rise time.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input. It is also suitable for use over both the industrial ($-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$) and automotive ($-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$) temperature ranges.

2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the automotive temperature range from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

3. Applications

- Automotive and industrial

4. Ordering information

Table 1. Ordering information

All types operate from -40°C to $+125^{\circ}\text{C}$

Type number	Package		
	Name	Description	Version
HEF4894BP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
HEF4894BT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
HEF4894BTT	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

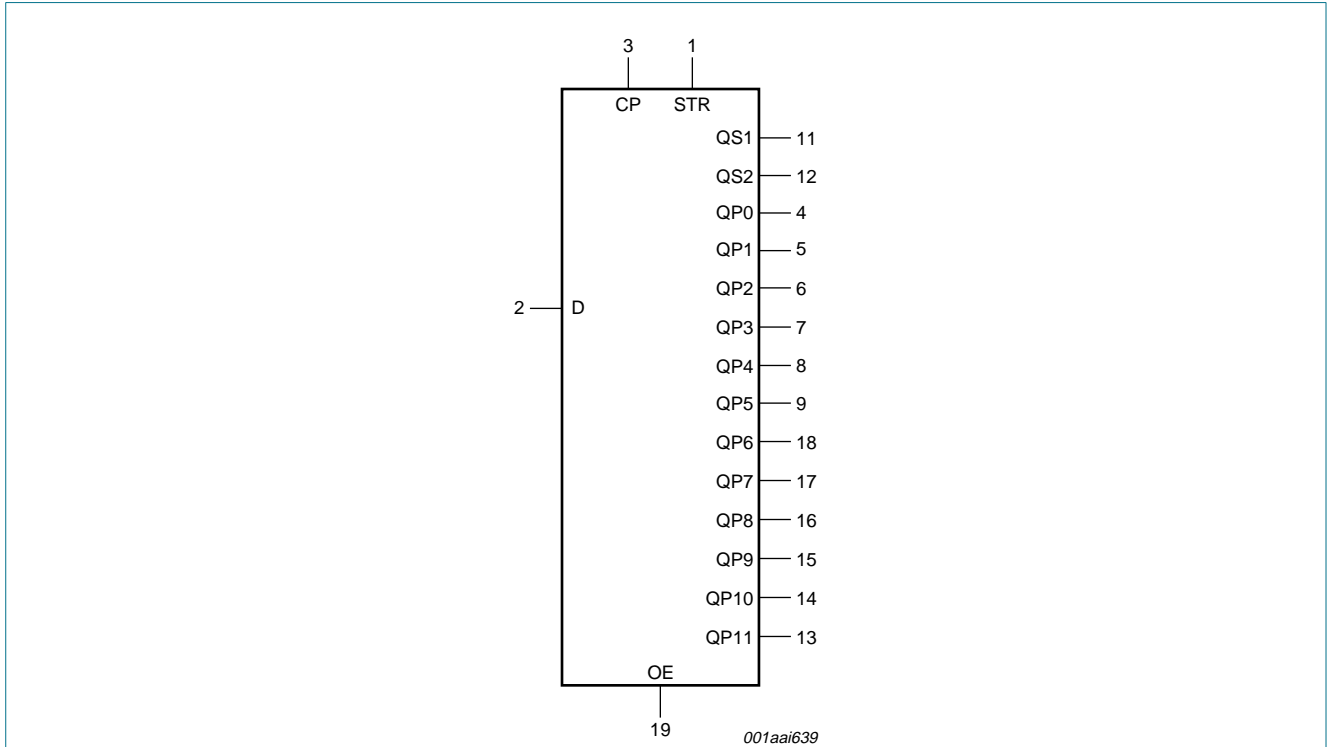


Fig 1. Logic Symbol

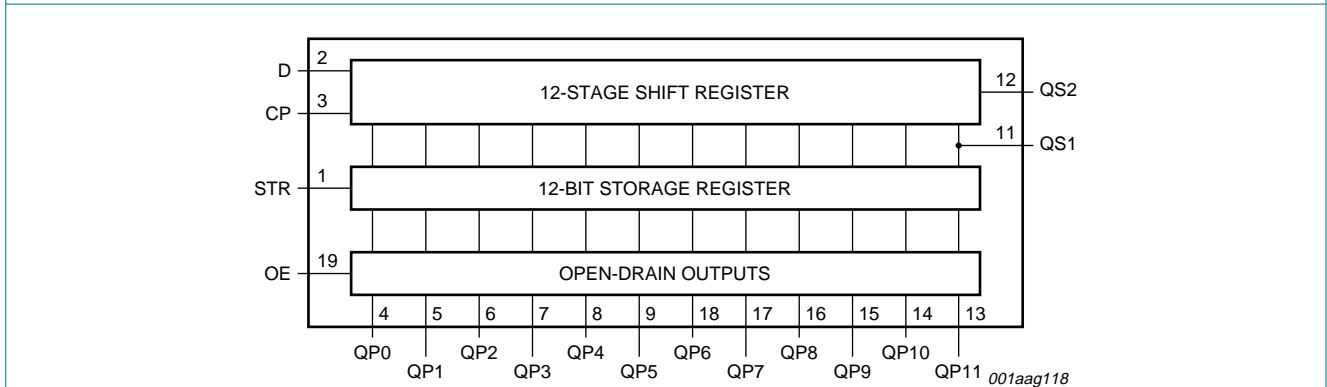


Fig 2. Functional diagram

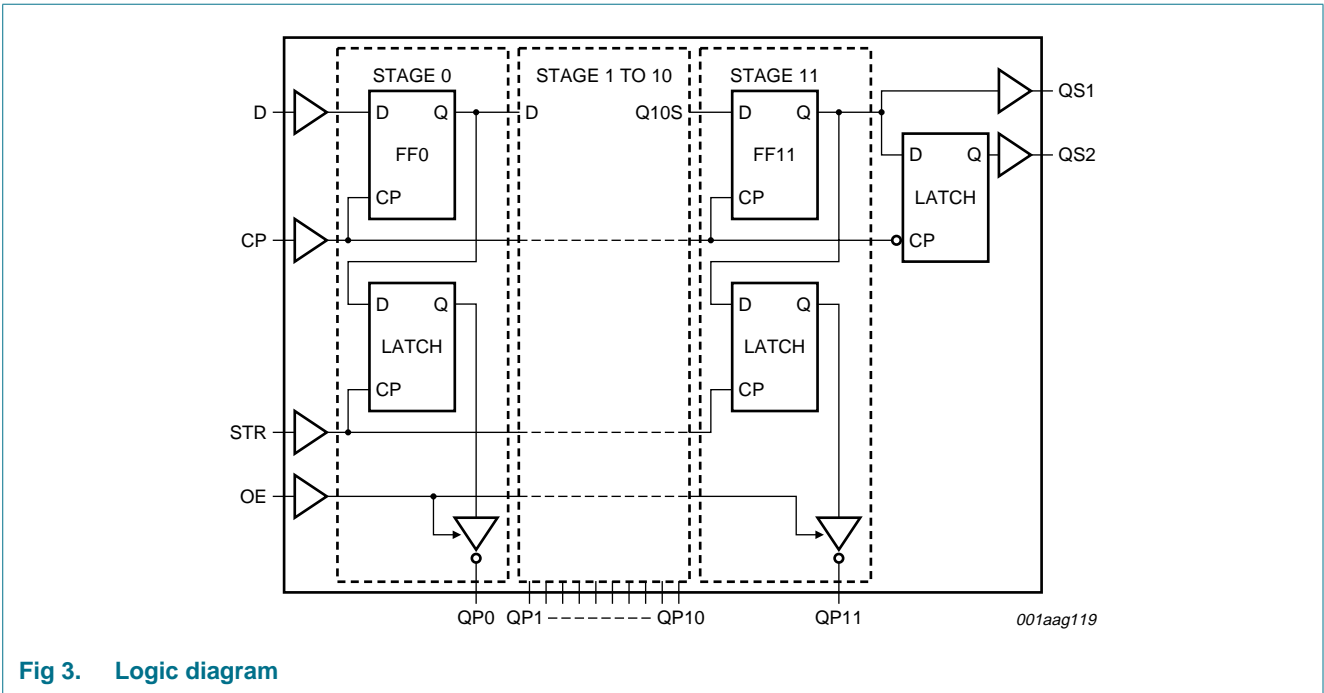


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

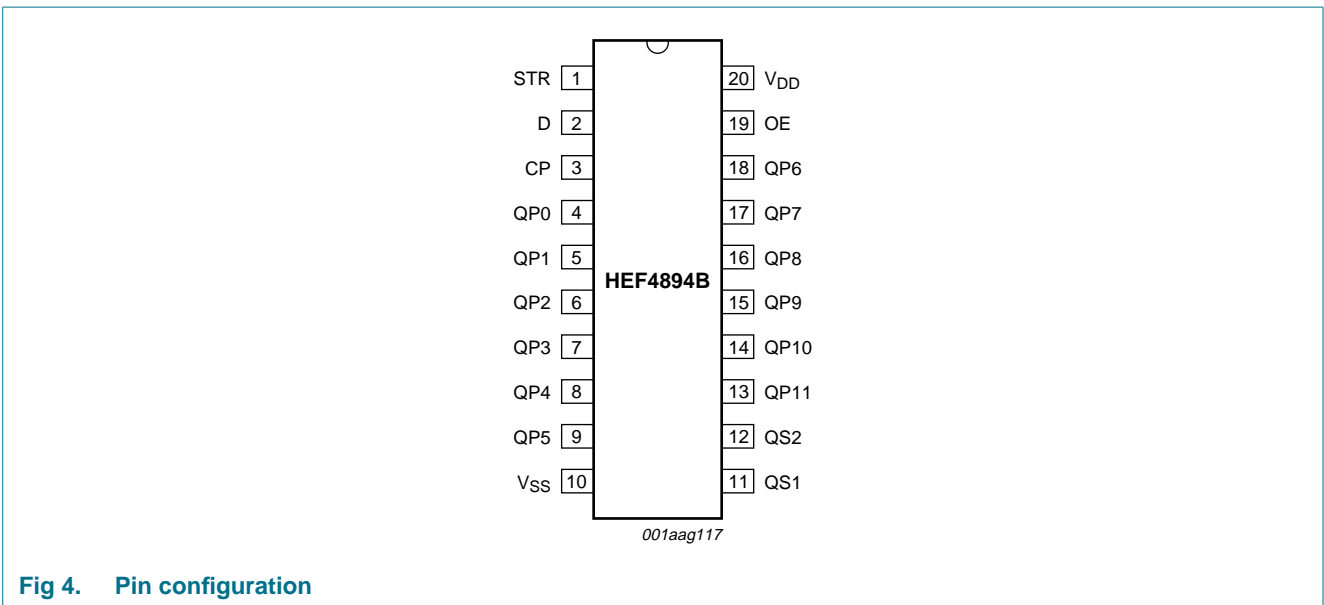


Fig 4. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
D	2	serial input
QP0 to QP11	4, 5, 6, 7, 8, 9, 18, 17, 16, 15, 14, 13	parallel output
QS1	11	serial output
QS2	12	serial output
CP	3	clock input
STR	1	strobe input
OE	19	output enable input
V _{DD}	20	supply voltage
V _{SS}	10	ground (0 V)

7. Functional description

Table 3. Function table^[1]

At the positive clock edge the information in the 10th register stage is transferred to the 11th register stage and the QS output

Control			Input	Parallel output		Serial output	
CP	OE	STR	D	QP0	QPn	QS1 ^[2]	QS2 ^[3]
↑	L	X	X	Z	Z	Q10S	no change
↓	L	X	X	Z	Z	no change	Q11S
↑	H	L	X	no change	no change	Q10S	no change
↑	H	H	L	Z	QPn-1	Q10S	no change
↑	H	H	H	L	QPn-1	Q10S	no change
↓	H	H	H	no change	no change	no change	Q11S

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition; Z = high-impedance OFF-state.

[2] Q10S = the data in register stage 10 before the LOW to HIGH clock transition.

[3] Q11S = the data in register stage 11 before the HIGH to LOW clock transition.

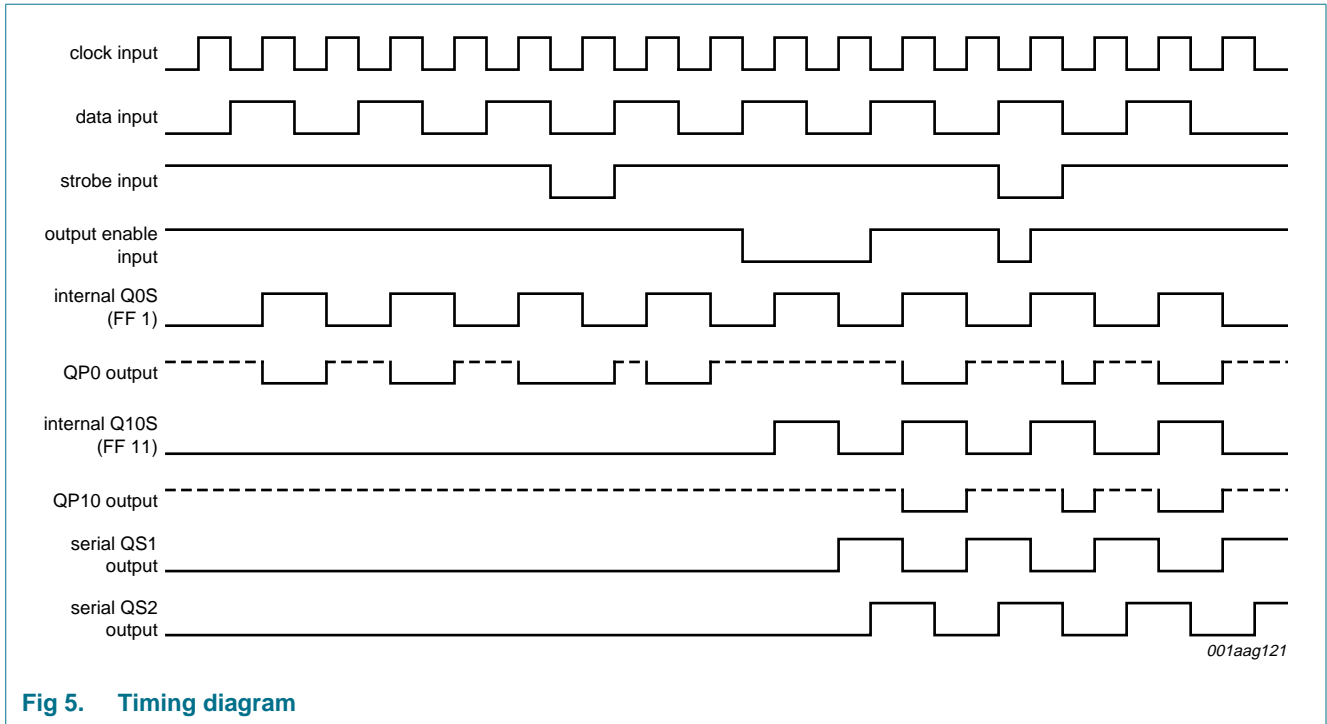


Fig 5. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < 0.5 \text{ V}$ or $V_I > V_{DD} + 0.5 \text{ V}$	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	QSn outputs; $V_O < 0.5 \text{ V}$ or $V_O > V_{DD} + 0.5 \text{ V}$	-	± 10	mA
		QPn outputs; $V_O < 0.5 \text{ V}$	-	40	mA
I_I	input leakage current		-	± 10	mA
I_O	output current	QSn outputs	-	± 10	mA
		QPn outputs	-	40	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+125	°C
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$			
		DIP20 package	[1] -	750	mW
		SO20 package	[2] -	500	mW
		TSSOP20 package	[3] -	500	mW
P	power dissipation		-	100	mW

[1] For DIP20 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO20 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For TSSOP20 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD}	supply voltage		3	-	15	V
V _I	input voltage		0	-	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	ns/V
		V _{DD} = 10 V	-	-	0.5	ns/V
		V _{DD} = 15 V	-	-	0.08	ns/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C		T _{amb} = +85 °C		T _{amb} = +125 °C		Unit	
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	HIGH-level input voltage	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V	
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V	
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V	
V _{IL}	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V	
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V	
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V	
V _{OH}	HIGH-level output voltage	QSn outputs; I _O < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V	
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V	
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V	
V _{OL}	LOW-level output voltage	QSn outputs; I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
		QPn outputs; I _O < 20 mA	5 V	-	0.75	-	0.75	-	1.5	-	1.5	V	
			10 V	-	0.75	-	0.75	-	1.5	-	1.5	V	
			15 V	-	0.75	-	0.75	-	1.5	-	1.5	V	
I _{OH}	HIGH-level output current	QSn outputs	V _O = 2.5 V	5 V	-1.7	-	-1.4	-	-1.1	-	-1.1	-	mA
			V _O = 4.6 V	5 V	-0.64	-	-0.5	-	-0.36	-	-0.36	-	mA
			V _O = 9.5 V	10 V	-1.6	-	-1.3	-	-0.9	-	-0.9	-	mA
			V _O = 13.5 V	15 V	-4.2	-	-3.4	-	-2.4	-	-2.4	-	mA
I _{OL}	LOW-level output current	QSn outputs	V _O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
			V _O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
			V _O = 1.5 V	15 V	4.2	-	3.2	-	2.4	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA	

Table 6. Static characteristics ...continued
 $V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = +25\text{ }^{\circ}\text{C}$		$T_{amb} = +85\text{ }^{\circ}\text{C}$		$T_{amb} = +125\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
I_{OZ}	OFF-state output current	QPn output is HIGH; $V_O = 15\text{ V}$	5 V	-	2	-	2	-	15	-	15	μA
			10 V	-	2	-	2	-	15	-	15	μA
			15 V	-	2	-	2	-	15	-	15	μA
I_{DD}	supply current	$I_O = 0\text{ A}$	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C_I	input capacitance		-	-	-	7.5	-	-	-	-	pF	

11. Dynamic characteristics

Table 7. Dynamic characteristics
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified. For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP to QS1; see Figure 6	5 V	[1] $132\text{ ns} + (0.55\text{ ns/pF})C_L$	-	160	320	ns
			10 V	$53\text{ ns} + (0.23\text{ ns/pF})C_L$	-	65	130	ns
			15 V	$37\text{ ns} + (0.16\text{ ns/pF})C_L$	-	45	90	ns
		CP to QS2; see Figure 6	5 V	$92\text{ ns} + (0.55\text{ ns/pF})C_L$	-	120	240	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF})C_L$	-	50	100	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
t_{PLH}	LOW to HIGH propagation delay	CP to QS1; see Figure 6	5 V	[1] $102\text{ ns} + (0.55\text{ ns/pF})C_L$	-	130	260	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
		CP to QS2; see Figure 6	5 V	$102\text{ ns} + (0.55\text{ ns/pF})C_L$	-	130	260	ns
			10 V	$49\text{ ns} + (0.23\text{ ns/pF})C_L$	-	60	120	ns
			15 V	$37\text{ ns} + (0.16\text{ ns/pF})C_L$	-	45	90	ns
t_{PZL}	OFF-state to LOW propagation delay	CP to QPn; see Figure 6	5 V		-	240	480	ns
			10 V		-	80	160	ns
			15 V		-	55	110	ns
		STR to QPn; see Figure 7	5 V		-	140	280	ns
			10 V		-	70	140	ns
			15 V		-	55	110	ns
t_{PLZ}	LOW to OFF-state propagation delay	CP to QPn; see Figure 6 and 7	5 V		-	170	340	ns
			10 V		-	75	150	ns
			15 V		-	60	120	ns
		STR to QPn; see Figure 7	5 V		-	100	200	ns
			10 V		-	40	100	ns
			15 V		-	35	70	ns

Table 7. Dynamic characteristics ...continued

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$ unless otherwise specified. For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit	
t_{en}		OE to QPn; see Figure 8	5 V	[2]	-	100	200	ns	
			10 V		-	55	110	ns	
			15 V		-	50	100	ns	
t_{dis}		OE to QPn; see Figure 8	5 V	[2]	-	80	160	ns	
			10 V		-	40	80	ns	
			15 V		-	30	60	ns	
t_t	transition time	QS1, QS2; see Figure 6	5 V	[1][3]		85	170	ns	
			10 V		$35\text{ ns} + (1.00\text{ ns/pF})C_L$	-	40	80	ns
			15 V		$19\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
t_W	pulse width	CP; LOW and HIGH; see Figure 6	5 V		60	30	-	ns	
			10 V		30	15	-	ns	
			15 V		24	12	-	ns	
		STR; HIGH; see Figure 7	5 V		80	40	-	ns	
			10 V		60	30	-	ns	
			15 V		24	12	-	ns	
t_{su}	set-up time	D to CP; see Figure 9	5 V		60	30	-	ns	
			10 V		20	10	-	ns	
			15 V		15	5	-	ns	
t_h	hold time	D to CP; see Figure 9	5 V		+5	-15	-	ns	
			10 V		20	5	-	ns	
			15 V		20	5	-	ns	
$f_{clk(max)}$	maximum clock frequency	CP; see Figure 6	5 V		5	10	-	MHz	
			10 V		11	22	-	MHz	
			15 V		14	28	-	MHz	

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

[2] t_{en} is the same as t_{PZL} and t_{dis} is the same as t_{PLZ} .

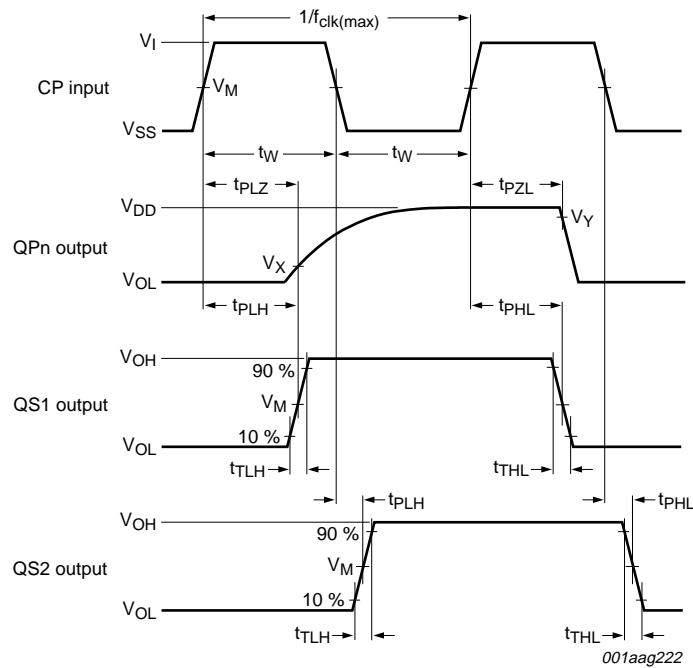
[3] t_t is the same as t_{TLH} and t_{THL} .

Table 8. Dynamic power dissipation

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	V_{DD}	Typical formula	Where
P_D	dynamic power dissipation	5 V	$P_D = 1200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\ \mu\text{W}$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.
		10 V	$P_D = 5550 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\ \mu\text{W}$	
		15 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\ \mu\text{W}$	

12. Waveforms

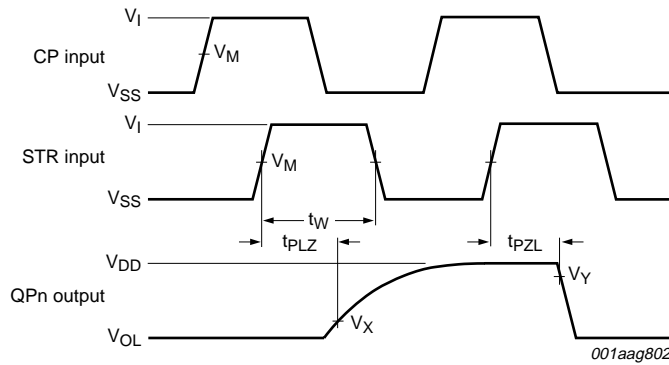


Parallel output measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. Propagation delay clock (CP) to output (QPn, QS1, QS2), clock pulse width and maximum clock frequency

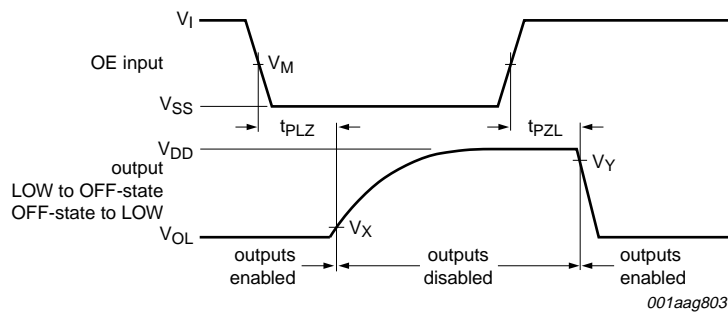
Table 9. Measurement points

Supply	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_O$	$0.9V_O$



Measurement points are given in [Table 9](#).
 V_{OL} is the typical output voltage level that occurs with the output load.

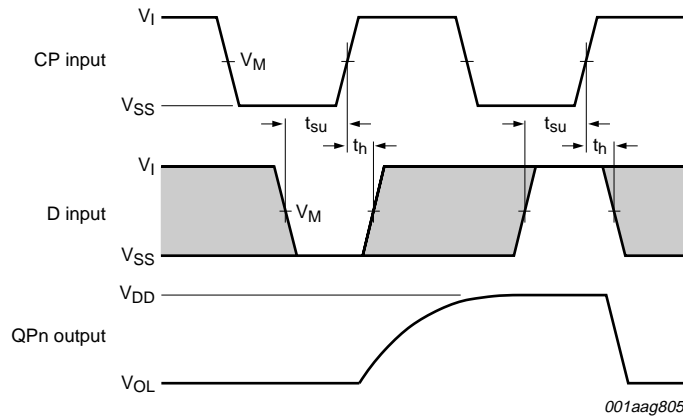
Fig 7. Strobe (STR) to output (QPn) propagation delays and the strobe pulse width



Measurement points are given in [Table 9](#).

V_{OL} is the typical output voltage level that occurs with the output load.

Fig 8. Enable and disable times for input OE

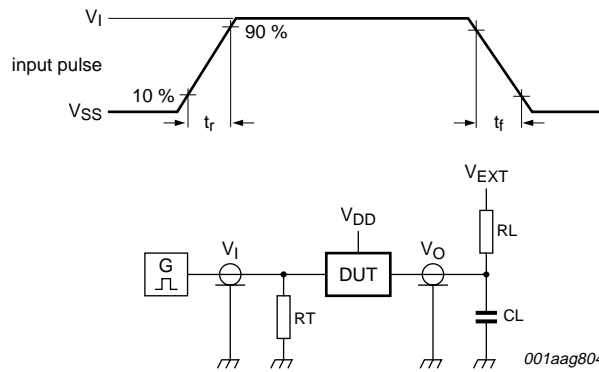


Measurement points are given in [Table 9](#).

V_{OL} is a typical output voltage level that occurs with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. Set-up and hold times for the data input (D)



Test data is given in [Table 10](#).

Definitions for test circuit:

DUT - Device Under Test;

R_L = Load resistance;

C_L = load capacitance;

R_T = Termination resistance should be equal to output impedance of Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

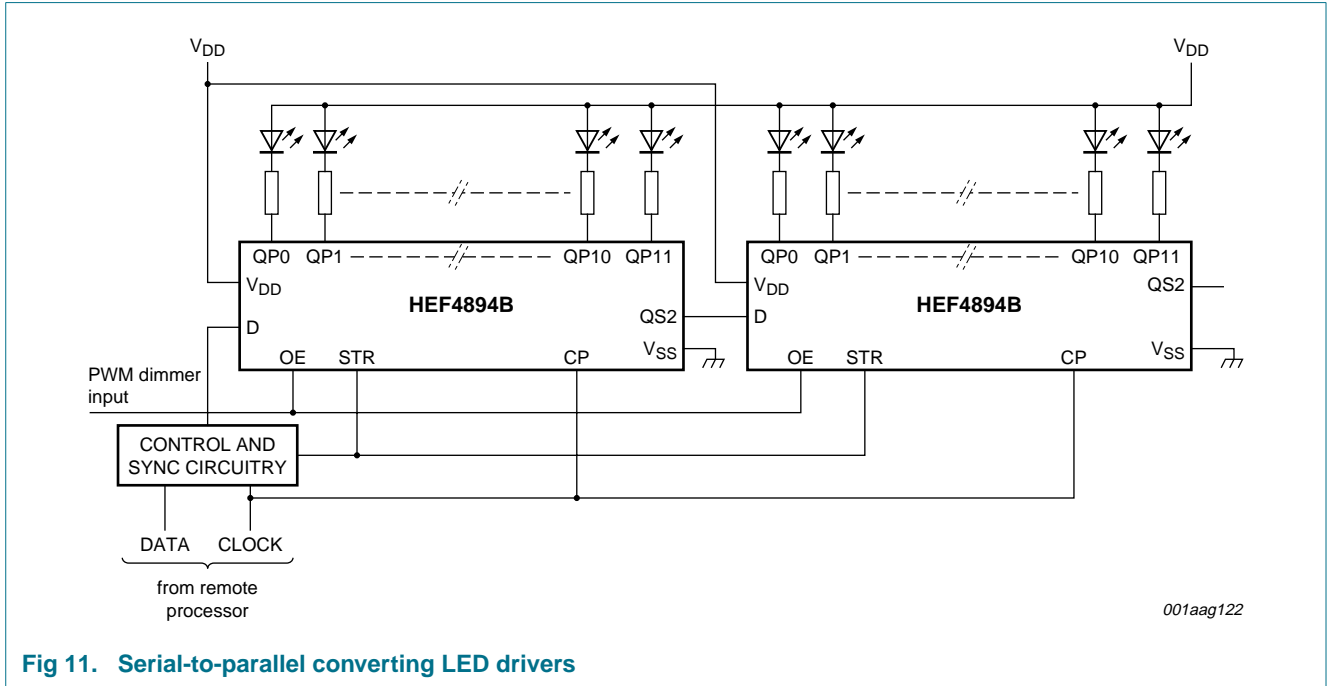
Fig 10. Test circuit for measuring switching times

Table 10. Test data

Supply	Input		V_{EXT}		Load	
V_{DD}	V_I	t_r, t_f	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}	C_L	R_L
5 V to 15 V	V_{DD}	≤ 20 ns	V_{DD}	open	50 pF	1 k Ω

13. Application information

Application example: serial-to-parallel data converting LED driver.



14. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

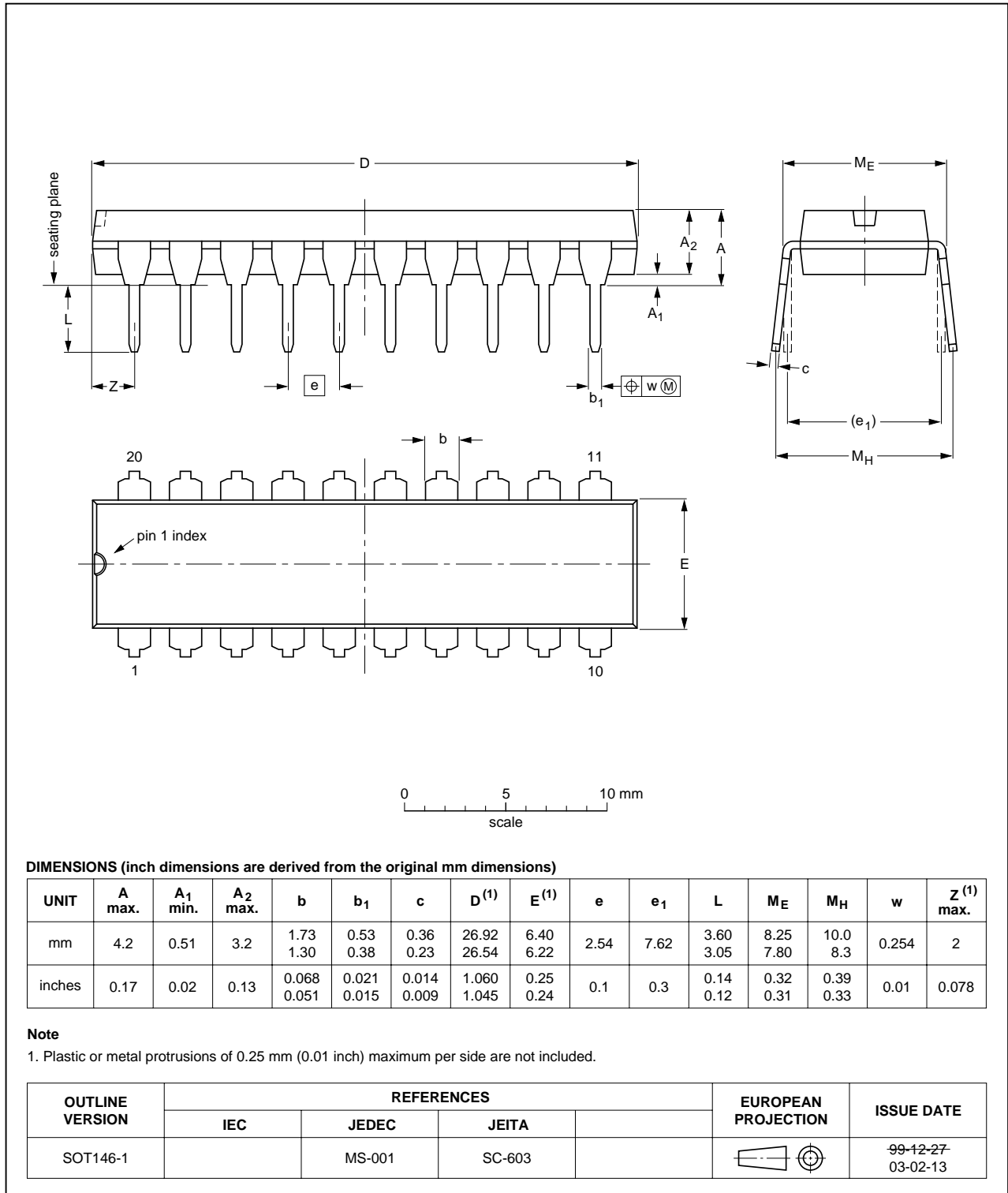


Fig 12. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

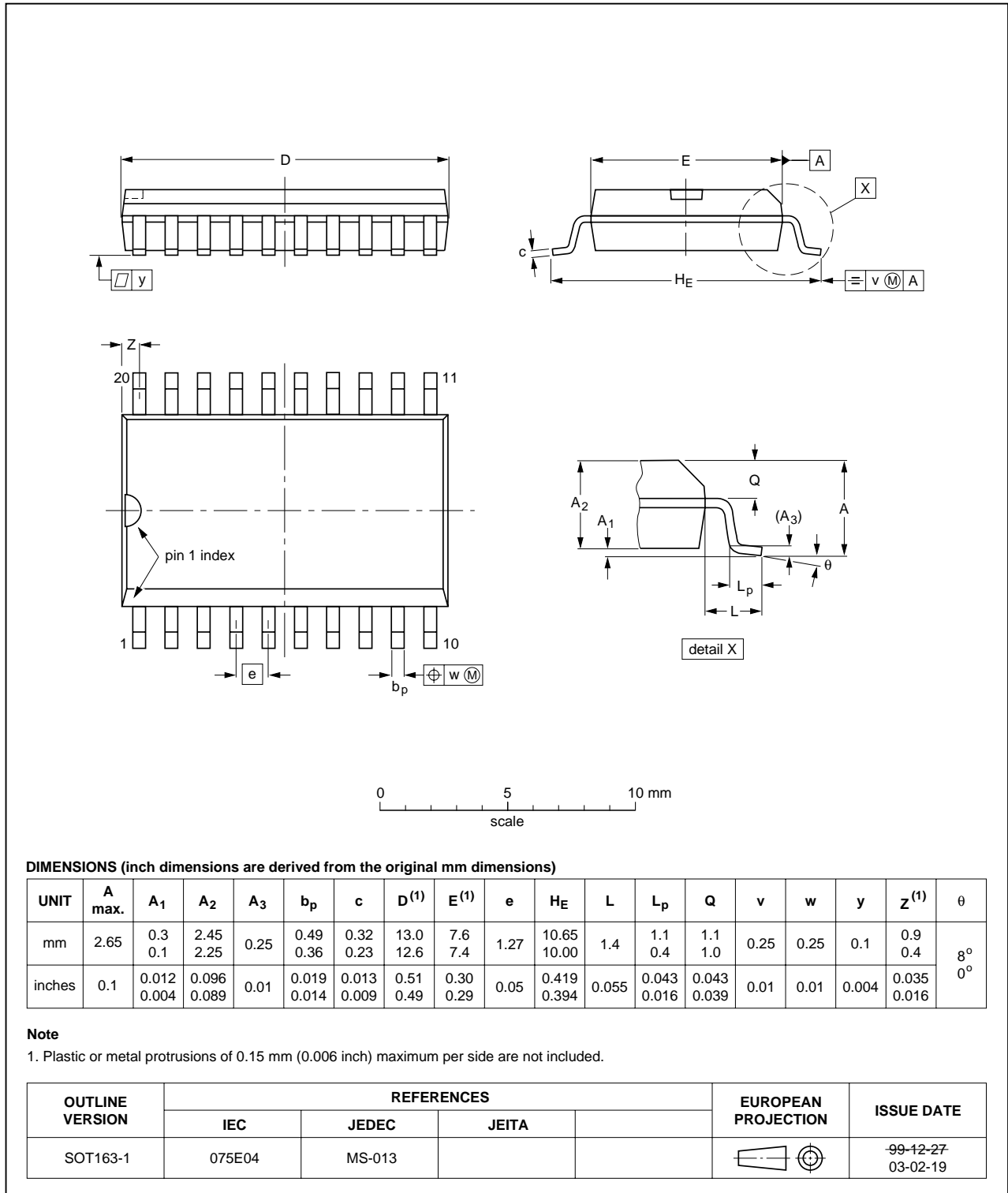


Fig 13. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

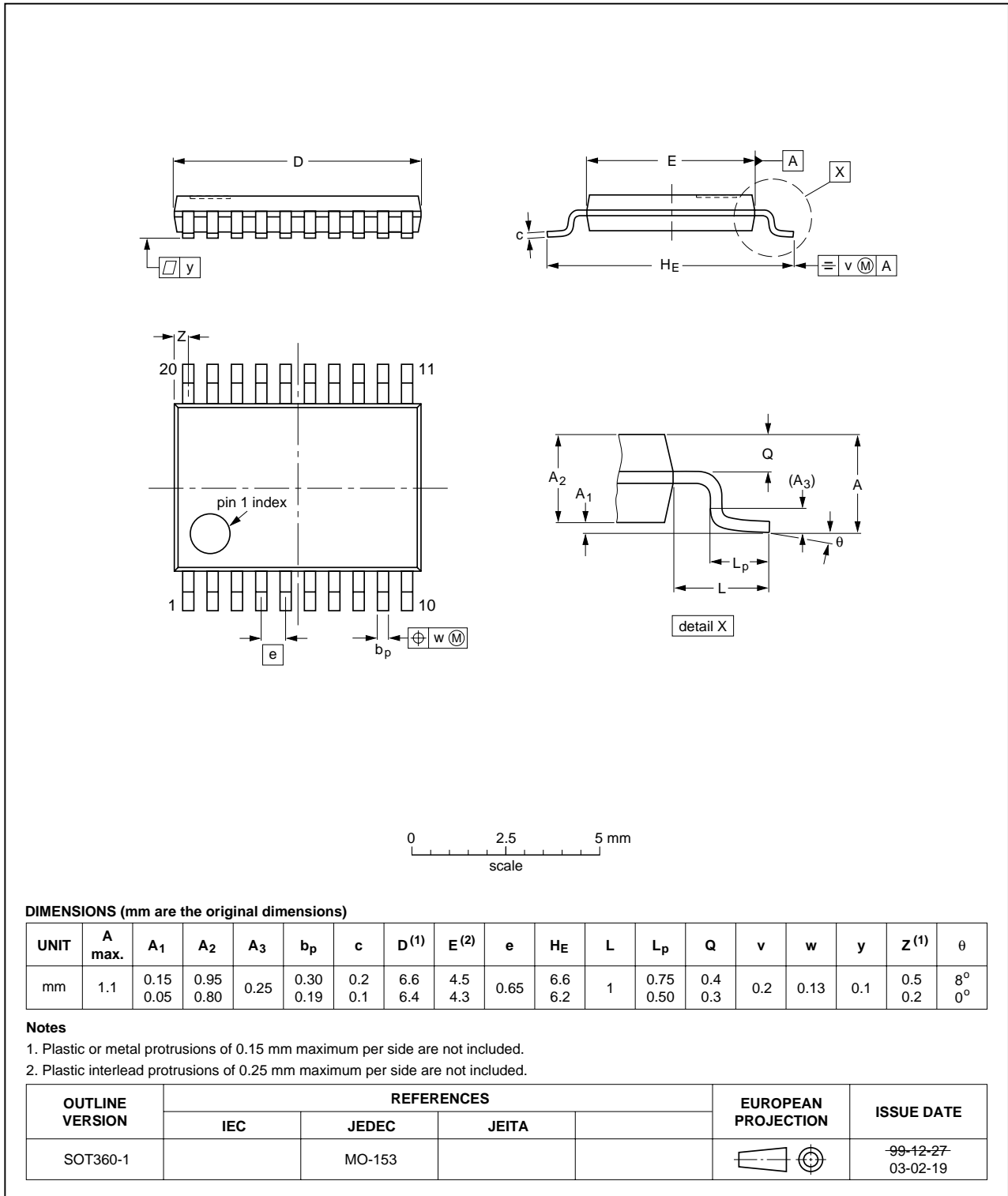


Fig 14. Package outline SOT360-1 (TSSOP20)

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4894B_4	20080827	Product data sheet	-	HEF4894B_CNV_3
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Temperature range maximum increased from 85 °C to 125 °C throughout the data sheet. • Pin names and descriptions modified throughout the data sheet. • Section 4 “Ordering information” and Section 14 “Package outline” TSSOP20 (SOT360-1) package added. • Figure 1 “Logic Symbol” added. • Table 4 “Limiting values”, Table 6 “Static characteristics” and Table 7 “Dynamic characteristics” reordered. • Figure 5 “Timing diagram” signals renamed. • Table 5 “Recommended operating conditions” added. • Section 8 “Limiting values”, Section 9 “Recommended operating conditions” and Section 10 “Static characteristics” added, taken from the HE4000B Family Specifications data sheet. • Section 10 “Static characteristics” I_{OH}, I_{OL}, I_I and I_{DD} values updated. • Section 10 “Static characteristics” Symbol C_I input impedance added. • Symbols t_{WCPL} and t_{WSTRH} renamed to t_W pulse width throughout the data sheet. • Symbols t_{en} and t_{dis} renamed to t_t transition time throughout the data sheet. • Symbol t_{hold} renamed to t_h hold time throughout the data sheet. • Symbol f_{max} renamed to $f_{clk(max)}$ maximum clock frequency throughout the data sheet. • Table 8 “Dynamic power dissipation” Symbol P changed to P_D dynamic power dissipation. • Typical temperature coefficient for propagation delays and output transitions removed. • Table 9 “Measurement points” and Table 10 “Test data” added. • Section 15 “Abbreviations” added. 			
HEF4894B_CNV_3	19950101	Product specification	-	HEF4894B_CNV_2
HEF4894B_CNV_2	19950101	Product specification	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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